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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BENGHUZZI, MOHSIN M	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/631,173	VILA ET AL.	
	Examiner	Art Unit	
	Mohsin (Ben) Benghuzzi	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *6 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-17, and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 7, and 23 have been considered but are moot in view of the new ground of rejection due to the amendment.

(1) Applicant's argument – {By contrast, Webb teaches "a parallel word of fixed value 10000000 is loaded into the shift register for recirculation. ... The word does not come from synchronization data from a transmitter ...} (Rejections under 35 U.S.C. § 102, page 9).

Examiner's response - Applicant's argument has been considered but is moot in view of the new ground of rejection of claim 7 over Webb et al. (US 4,855,735) in view Wilkinson (US 4,543,657), which was necessitated by the amendment. Wilkinson discloses a receiver wherein a pseudo random number, i.e., a word comes from synchronization data from a transmitter (Column 2, lines 41-44 and lines 50-52).

(2) Applicant's argument – {Thus Wilkinson does not teach identifying "the occurrence of errors such that the integrity of the communications link can be continually monitored."} (Rejections under 35 U.S.C. § 103, paragraph 7, page 11).

Examiner's response - Applicant's argument has been considered but is moot in view of the new ground of rejection of claim 1 over Webb et al. (US 4,855,735) and Wilkinson (US 4,543,657), and further in view of Dulaney et al. (US 3,916,379), which was necessitated by the amendment. Dulaney et al. teaches a method comprising

identifying occurrence of errors such that the integrity of the communications link can be continually monitored (Abstract, lines 1-3 and column 2, lines 31-34).

(3) Applicant's argument – {Applicant respectfully submits that the present invention is nonobvious in light of Webb and Wilkinson at least because neither Webb or Wilkinson teach: "wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors such that the integrity of the communications link can be continually monitored."} (Rejections under 35 U.S.C. § 103, paragraph 4, page 11).

Examiner's response - Applicant's argument has been considered but is moot in view of the new ground of rejection of claim 1 over Webb et al. (US 4,855,735) and Wilkinson (US 4,543,657), and further in view of Dulaney et al. (US 3,916,379), which was necessitated by the amendment. Wilkinson does teach a method wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter (Column 2 Lines 41-47 and Column 3 Lines 19-32). Regarding the integrity of the communications link being continually monitored, Dulaney et al. discloses a receiving system wherein the integrity of the communications link is continually monitored (Abstract, lines 1-3 and column 2, lines 31-34).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7-17, 19-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al. (US 4,855,735) in view of Wilkinson (US 4,543,657), and further in view of Dulaney et al. (US 3,916,379).

1) Regarding claim 1:

Webb et al. teaches a method comprising:

receiving one or more bits of synchronization data from a transmitter in a receiver of a communications link (Column 4 Lines 16-18);

loading the one or more bits of synchronization data into a shift register in the receiver, wherein the receiver shift register has a feedback circuit (Column 5 Lines 12-15);

if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register (Column 5 Lines 3-13 and Column 6 Lines 40-41); and

if the receiver shift register is not filled with synchronization data, shifting the loaded synchronization data and loading one or more additional bits of synchronization data into the receiver shift register (Column 5 Lines 25-29 and Column 2 Lines 64-68).

Webb et al. does not teach, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors; however, Wilkinson teaches one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors (Column 2 Lines 41-47 and Column 3 Lines 19-32).

It is desirable that occurrence of error and its frequency in a received sequence be determined. This determines the bit error rate of the channel, and therefore, reliability of received data (See Wilkinson, Column 3 Lines 22-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the method of identifying the occurrence of errors, as Wilkinson teaches, into the method of Webb et al., in order to determine the bit error rate of the channel, and therefore, reliability of received data.

Webb et al. or Wilkinson do not teach the integrity of the communications link can be continually monitored; however, Dulaney et al. discloses a receiving system wherein the integrity of the communications link is continually monitored (Abstract, lines 1-3 and column 2, lines 31-34).

It is desirable that the integrity of a communication link is continually monitored. Continual monitoring of a communication link allows for the detection of any malfunction or degradation of the link and, thus, allows for timely corrective actions to be instituted (See Dulaney et al. column 1, lines 32-36). Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to have the integrity of Webb et al. and Wilkinson be continually monitored, as Dulaney et al. teaches, in order to be able to detect any malfunction or degradation and, thus, allow for the institution of timely corrective actions.

2) Regarding claim 2:

Webb et al. teaches, wherein receiving one or more bits of synchronization data comprises receiving idle codes containing synchronization data (Column 4 Lines 16-18 and Column 6 Lines 37-41, wherein, successive logical one data bit is interpreted to be the idle codes).

3) Regarding claim 3:

Webb et al. teaches, further comprising determining whether the receiver shift register is filled with synchronization data by counting a predetermined number of cycles after a reset even (Column 5 Lines 12-21).

4) Regarding claim 4:

Webb et al. teaches, wherein the receiver shift register comprises a plurality of serially coupled flip-flops, and wherein shifting the loaded synchronization data comprises shifting the bit in each flip-flop to a next flip-flop (Column 4 Lines 29-31, Column 3 Lines 11-12, and Column 5 Lines 7-13, wherein, it is understood that recirculation is propagation of a bit from one flip-flop of the shift register to another).

5) Regarding claim 5:

Webb et al. teaches, wherein loading the one or more additional bits of synchronization data into the receiver shift register comprises loading the one or more

additional bits of synchronization data into one or more predetermined cells of the receiver shift register (Column 5 Lines 12-15).

6) Regarding claim 7:

Webb et al. discloses a system comprising:

a receiver shift register (40 in Fig. 1 and Column 4 Lines 18-19); and

a feedback circuit coupled to the receiver shift register (Column 6 Lines 42-48, wherein, 'output means being connected to the input means for recirculating data bits' is interpreted as equivalent to the feedback circuit);

wherein one or more cells of the receiver shift register are configured to alternatively accept as input either a bit from a preceding cell or a received bit of synchronization data from a transmitter (Column 5 Lines 25-29 and Lines 7-21), and

wherein if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register (Column 5 Lines 3-13 and Column 6 Lines 40-41).

Furthermore, as discussed in claim 1 above, Wilkinson discloses, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors.

Regarding the integrity of the communications link being continually monitored, as discussed in claim 1 above, Dulaney et al. discloses a receiving system wherein the integrity of the communications link is continually monitored (Abstract, lines 1-3 and column 2, lines 31-34).

7) Regarding claim 8:

Wilkinson discloses, further comprising a counter coupled to the receiver shift register, wherein the counter is configured to assert a "synchronized" signal when a predetermined count is reached after a reset event (Column 6 Lines 36-41).

8) Regarding claim 9:

Wilkinson further discloses, wherein the predetermined count corresponds to the receiver shift register being filled with synchronization data (Column 6 Lines 36-43, wherein, "Fill" is equivalent to filled with synchronization data).

9) Regarding claim 10:

Webb et al. discloses, wherein the one or more cells of the receiver shift register are configured to accept received bits of synchronization data as input until the receiver shift register is filled with synchronization data, and to accept bits from preceding cells as input when the receiver shift register is filled with synchronization data (Column 5 Lines 3-21, Column 4 Lines 29-31, and Column 3 Lines 11-12, wherein, it is understood that recirculation is propagation of a bit from one flip-flop of the shift register to another).

10)Regarding claim 11:

Webb et al. discloses, wherein upon occurrence of a reset event, data in the receiver shift register is invalid data (Column 4 Lines 58-60).

11)Regarding claim 12:

Wilkinson further discloses, further comprising one or more demultiplexers coupled to provide input to the one or more cells, wherein the one or more

demultiplexers are configured to select either bits from preceding cells or received bits of synchronization data to provide as input to the one or more cells (Column 2 Line 64 to Column 3 Line 2, wherein, switching means is interpreted as demultiplexers, and shift register comprises preceding cells, as discussed above).

12)Regarding claim 13:

Wilkinson further discloses, wherein the demultiplexers are coupled to receive an indication of whether the receiver shift register is synchronized (Column 2 Lines 61-63).

13)Regarding claim 14:

Wilkinson further discloses, wherein the demultiplexers are coupled to a counter, wherein the counter is configured to provide the indication when a predetermined count is reached after a reset event (Column 6 Lines 36-41).

14)Regarding claim 15:

Webb et al. discloses, further comprising a transmission medium coupled to the receiver shift register (Column 3 Lines 50-52 and in Fig. 1 'PARALLEL DATA WORD' coupled to the shift register 40).

15)Regarding claim 16:

Webb et al. discloses, wherein the transmission medium is configured to transport the synchronization data in idle codes (Column 7 Lines 17-20, wherein, the data clock signal is interpreted as the idle codes. Also, see claim 15 above).

16)Regarding claim 17:

Wilkinson further discloses, wherein the transmitter shift register configured to generate a first bit sequence, and the receiver shift register is configured to generate an identical bit sequence (Column 6 Lines 1-6 and Column 11 Lines 38-41).

17)Regarding claim 19:

Webb et al. discloses the system of claim 7, wherein the receiver shift register is configured to load synchronization data on each cycle into one or more predetermined cells of the receiver shift register (Column 8 Lines 1-8).

18)Regarding claim 20:

Webb et al. discloses the system of claim 19, wherein the one or more predetermined cells of the receiver shift register exclude at least one of the cells of the receiver shift register (Column 3 Lines 54-58 and Column 6 Lines 42-48, wherein, when number of bits n is chosen to be greater than the number of bits in the converted 8 bit binary number, i.e., when n is chosen to be 9 or greater, predetermined cells will exclude at least one of the cells of the receiver shift register).

19)Regarding claim 21:

Webb et al. discloses the system of claim 20, wherein the receiver shift register cells comprise 11 serially coupled flip-flops and wherein the predetermined cells comprise 8 consecutive ones of the 11 serially coupled flip-flops (Column 3 Lines 54-58 and Column 6 Lines 42-48, wherein, n is chosen to be 11).

20)Regarding claim 23:

Webb et al. discloses a system comprising:

a receiver shift register (40 in Fig. 1 and Column 4 Lines 18-19); and

a feedback circuit coupled to the receiver shift register (Column 6 Lines 42-48, wherein, 'output means being connected to the input means for recirculating data bits' is interpreted as equivalent to the feedback circuit);

wherein one or more cells of the receiver shift register are configured to initially alternatively accept as input a received bit of synchronization data from a transmitter and, upon receiving an indication that the receiver shift register is synchronized with the transmitter, accept as input a bit from a preceding cell (Column 5 Lines 7-21 and Lines 25-29), and

wherein if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register (Column 5 Lines 3-13 and Column 6 Lines 40-41).

Furthermore, as discussed in claim 1 above, Wilkinson discloses, wherein during synchronized operation, one or more bit sequences generated by the receiver shift register are compared to a plurality of received bit sequences interspersed in a transmission from the transmitter to identify the occurrence of errors.

Regarding the integrity of the communications link being continually monitored, as discussed in claim 1 above, Dulaney et al. discloses a receiving system wherein the integrity of the communications link is continually monitored (Abstract, lines 1-3 and column 2, lines 31-34).

4. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al. (US 4,855,735), Wilkinson (US 4,543,657), Dulaney et al. (US 3,916,379), and further in view of Nozuyama (US 5,867,409).

Webb et al., Wilkinson, or Dulaney et al. do not disclose, wherein the feedback circuit comprises an exclusive OR (XOR) gate having two inputs coupled to receive the outputs of two of the cells of the receiver shift register, the XOR gate further having an output that is coupled to the input of a first cell of the receiver shift register. However, Nozuyama discloses, wherein the feedback circuit comprises an exclusive OR (XOR) gate having two inputs coupled to receive the outputs of two of the cells of the receiver shift register, the XOR gate further having an output that is coupled to the input of a first cell of the receiver shift register (30 in Fig. 3, wherein, XOR gate output is coupled to flip-flop 1).

It is essential that an XOR gate be used in Webb et al.'s feedback register. Use of the XOR gate allows the formation of two or more flip-flops in the feedback circuit (See Nozuyama, Column 5 Lines 43-46). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an XOR gate, as Nozuyama teaches, in the feedback circuit of Webb et al., Wilkinson, and Dulaney et al., in order to allow the formation of two or more flip-flops.

Conclusion

5. Applicant's amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kanasugi et al. (US Pub 2003/0046636) discloses an error detector at a receiver comprising a feedback shift register, with the transmitter also having the same, but with a shift direction that is opposite in direction.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached on 8:30- 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mohsin (Ben) Benghuzzi May 13, 2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER